Northeast Semiconductor, Inc.

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February 29, 1992

Dr. Erhard Schimitschek, Scientific Officer
ATTN: Code 808
REF: N00014-91-C-0222
Naval Ocean Systems Center
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San Diego, CA 92152-5000

Re:	Contractor	:	Northeast Semiconductor, Inc.
	Address	:	767 Warren Road, Ithaca, NY 14850
	Req. No.	:	s405811srv02/17 APR
	Contract No.	:	N00014-91-C-0222
	Report Date	:	November 26, 1991
	Report Title	:	Third Monthly Technical Report
	Period Covered	:	02/01/92 through 02/29/92

Dear Dr. Schimitschek:

Northeast Semiconductor, Inc. encloses its Third Monthly Technical Report (Line Item #0002) pursuant to the provisions of contract Section B entitled, "Supplies or Services and Prices/Costs" for the period of February 1, 1992 through February 29, 1992.

Innovative Techniques for the Production of Low Cost 2D Laser Diode Arrays

1.0 OBJECTIVE

The primary objective of this program is to develop a low cost, high yielding methodology for processing, packaging and characterization of MBE grown two dimensional high power laser diode arrays. Projected increases in overall yield of AlGaAs diode lasers would reduce manufacturing cost from the current $10 to $20 per peak watt to below $3 per peak watt. Emphasis will be placed on innovative packaging techniques that will utilize recent advances in diamond heat sinking technology.

2.0 PROGRAM METHOD AND SCHEDULE

This program consists of four phases which will demonstrate reduced manufacturing cost and improved device performance of NSI's MBE laser diode arrays. The four phases listed below will result in milestones in processing, packaging, and testing along with delivery of the specified number of 5-bar laser arrays.

(i) Concept phase: Conceptual design and organization of this phase II program. NSI will utilize the current side cooled strained relief package to manufacture 5-bar laser diode arrays for base line evaluation. (Deliverables: 3 5-bar arrays.)

(ii) Backplane phase: Development of a copper backplane cooling technology that incorporates CVD diamond submounts. This phase will also include the completion of room temperature photoluminescence development. (Deliverables: 5 5-bar arrays.)

(iii) Diamond Backplane phase: Develop a CVD diamond backplane cooling scheme that will utilize smaller CVD submounts. The reduction in submount size is to decrease the thermal resistance from the laser bar to the backplane. (Deliverables: 5 5-bar arrays.)

(iv) Liquid Cooled Submount phase: An innovative liquid cooled package will be developed. The CVD diamond submounts will be hermetically sealed, electrically isolated and liquid cooled. (Deliverables: 5 5-bar arrays.)

The following global issues not mentioned above will be investigated continuously throughout all four phases of this program:

(1) design and development of a mask set to increase processing and packaging yields,

(2) development and updating of MBE growth software,

(3) design and development of an in-house facet coating station,

(4) evaluation of different facet coating materials,

(5) development of automated tests,

(6) life test and burn-in development.

The master schedule for this program is shown in Table 1. Each phase will require wafer growth, processing, assembly and test. The schedule shows the estimated number of sample fabrications and tests, as well as the time of hardware deliverables and reports.

3.0 PROGRESS THIS PERIOD

3.1 Wafer Growths

A total of four 2 inch wafers were grown for this program last month. Arsenic flux and aluminium percentage calibration experiments were performed, under a related contract, to achieve the desired wavelength and maximum PL intensities. The two wafers, shown in figure #1, provided PL wavelengths of 795nm to 800nm and moderate PL intensities. These wafers are currently being processed, and should produce 808nm pulsed laser diode arrays.

3.2 Processing

The new mask set designed for this program has arrived. Advantages of this mask set include, extensive test structures aimed at pre-packaging evaluation, the ability to utilize photosensitive polyamide to reduce chance of current leakage, and reduction in the number of processing steps. Wafer number M21362 is currently being processed and will utilize this new mask set.

Efforts continue on solving facet coating problems. Last period work was done to eliminate shadowing of the facets by two procedural changes. The first was to perform the deposition of the coatings with the holding jig stationary and tilted slightly, instead of rotating, to minimize shadowing due to misalignment. The other change involved detailed inspections of the laser diode and dummy (separation) bars for plane jumping during cleaving. Initial trails resulted in inferior coatings. Modifications were then made to guarantee the quality of the coatings by recalibration of the system and tooling factor to account for the stationary position. A recent facet coating run, after recalibrating, is currently being evaluated.

Investigation of different front facet coating materials continued. Life test data is being collected on arrays with TiO_2 and Ta_2O_5 as a front facet alternative. These arrays are tested in nitrogen and air to determine the sensitivity of the coatings to moisture. Figure #2 A&B show life test data for arrays with TiO_2, and Ta_2O_5 coatings respectively. The TiO_2 array in nitrogen showed less degradation over 2×10^8 pulses but then failed catastrophically. This failure is believed to be associated with device current leakage detected at the start of the test. The array in air has over 7.4×10^8 pulses with a degradation of 23%. An array with Ta_2O_5 as a coating is being tested in air and is showing a 8% power degradation over 1.2×10^8 pulses. Additional data needs to be gathered on these different coatings before any conclusions can be made.

3.3 Testing

Recent developments in PL measurements include increasing the number of points scanned across the radial distance of the wafer. This action was prompted by the need to sufficiently characterize the uniformity of the wafer and define optimal areas to process. The slits in the monochromator were also reduced from 500μm to 300μm to increase resolution of the spectrum for each scan.

Software upgrades to life test programs continued this period. The background data acquisition programming was completed, improving the reliability and flexibility of the programs. Development work is presently underway for live screen monitoring and menu driven selections.

Life test capability is currently limited by the number of drive pulsers available. A prototype of NSI's pulser is completed and is currently testing an array for front facet coat evaluations for this program. A voltage ripple appearing on the output waveform was found to be cause by insufficient charging of the capacitor bank. This problem was corrected by installing a higher secondary voltage power transformer into the pulser unit.

3.4 Assembly and Packaging

Experiments in evaporating different composition solders took place this period. 70%In/30%Pb, 75%Pb/25%In, and 50%In/50%Sn composition solders were investigated. The 70%In/30%Pb proved the most promising. The deviation from 100%In was prompted by two reasons. The first being the low melting point of pure In causing problems with step soldering that will be needed for backplane cooling models. The second pertains to the increased strength of the solder joint between the submount and laser diode bar for 70%In/30%Pb. Evaporation of 5μm to 7μm of this solder has been readily reproducible, and over 25 arrays have been successfully fabricated. Results on 75%Pb/25%In evaporations are encouraging. However, due to the higher temperatures involved and longer solder cycle times, NSI will utilize the 70%In/30%Pb composition. Preliminary findings on co-evaporation of 50%In/50%Sn solder indicates difficulties with excessive temperatures and uncontrolled deposition rates. An alternative approach will be to evaporate the InSn in separate layers.

CVD diamond is continually being investigated. Sample pieces from the manufacturer have not yet arrived but are expected early next month. Development has taken place on backplane metalization schemes as well as grooved diamond. The grooved diamond can be manufactured by either laser cutting the slits or by growing diamond on pattern silicon wafers. Both methods are being investigated to determine the most feasible approach.

4.0 PLANS FOR MARCH

Investigation will continue on pressing issues such as facet coating, increased life test capability, and improved packaging yields. Efforts will be placed on evaluation of the new mask set on wafers currently being processed, and on CVD diamond as a heat sink alternative.

Delivery of three 5-bar arrays with NSI's standard side cooled package will be completed by the end of March. These deliverables will serve as a base line evaluation during this program.

Very truly yours,

Michael J. Cook,
Principal Investigator
Northeast Semiconductor, Inc.

:nd
Encl: 1 Copy of 3rd Monthly Technical Report

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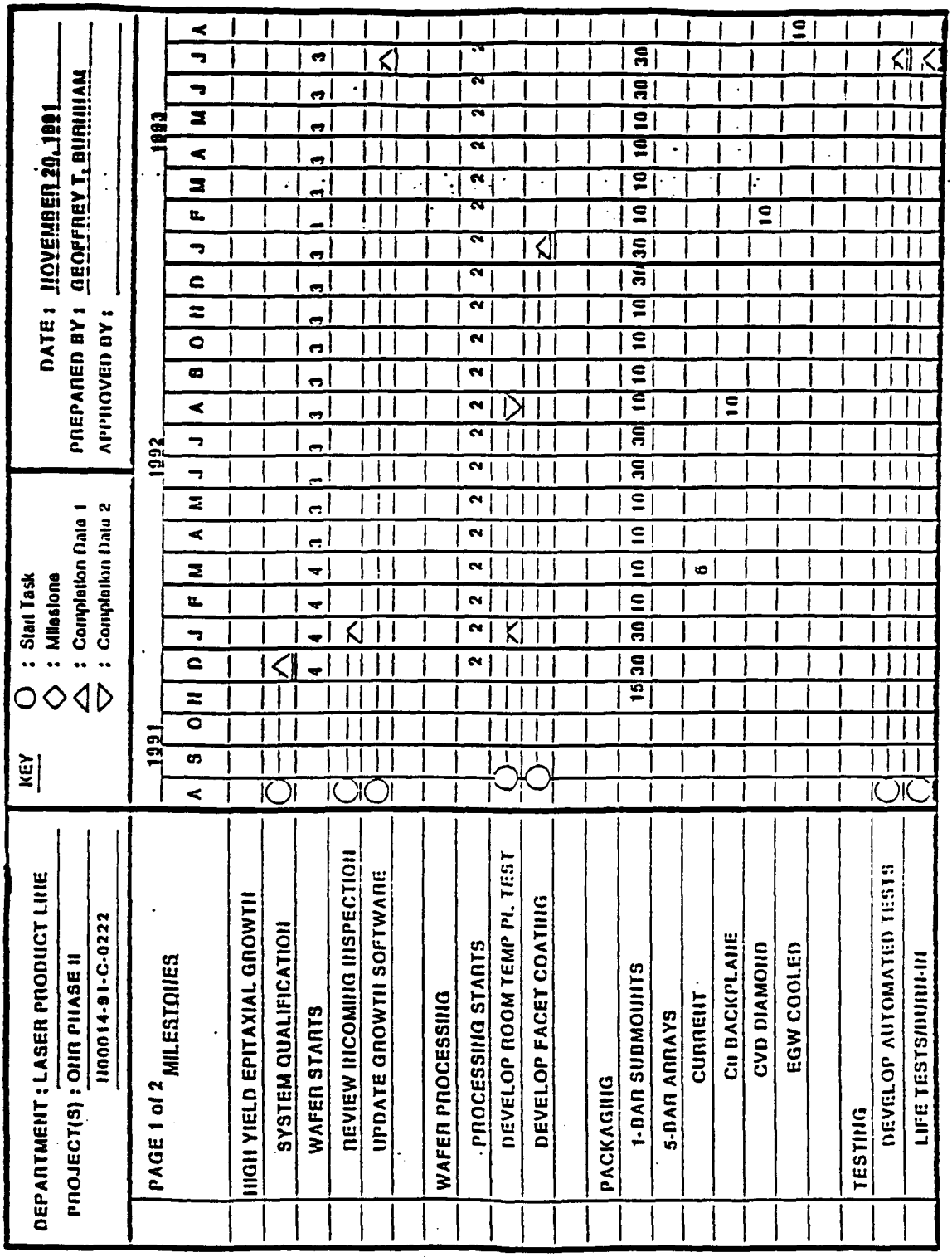
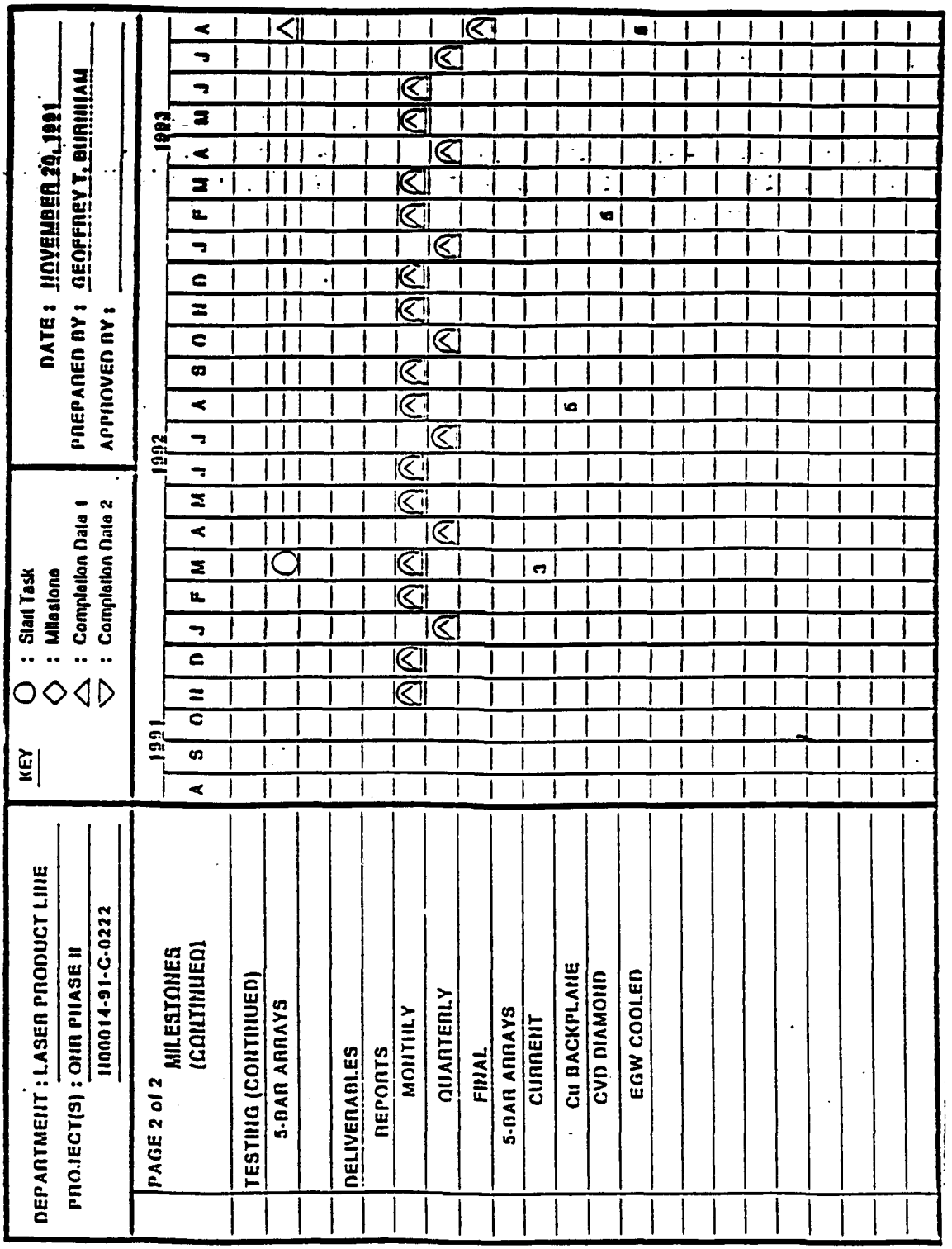


TABLE 1. MASTER SCHEDULE FOR SBIR PHASE I
CONTRACT NO. N00014-91-C-0222


DEPARTMENT : LASER PRODUCT LINE
PROJECT(S) : ONR PHASE II
N00014-91-C-0222
KEY
○ : Start Task
◇ : Milestone
◁ : Completion Date 1
▷ : Completion Date 2
DATE : NOVEMBER 20, 1991
PREPARED BY : GEOFFREY T. BURNHAM
APPROVED BY :
PAGE 2 of 2
MILESTONES
(CONTINUED)
1991
1992
1993
A S O N D J F M A M J J A S O N D J F M A M J J A
TESTING (CONTINUED)
5-BAR ARRAYS
DELIVERABLES
REPORTS
MONTHLY
QUARTERLY
FINAL
5-BAR ARRAYS
CURRENT
Cu BACKPLANE
CVD DIAMOND
EGW COOLED

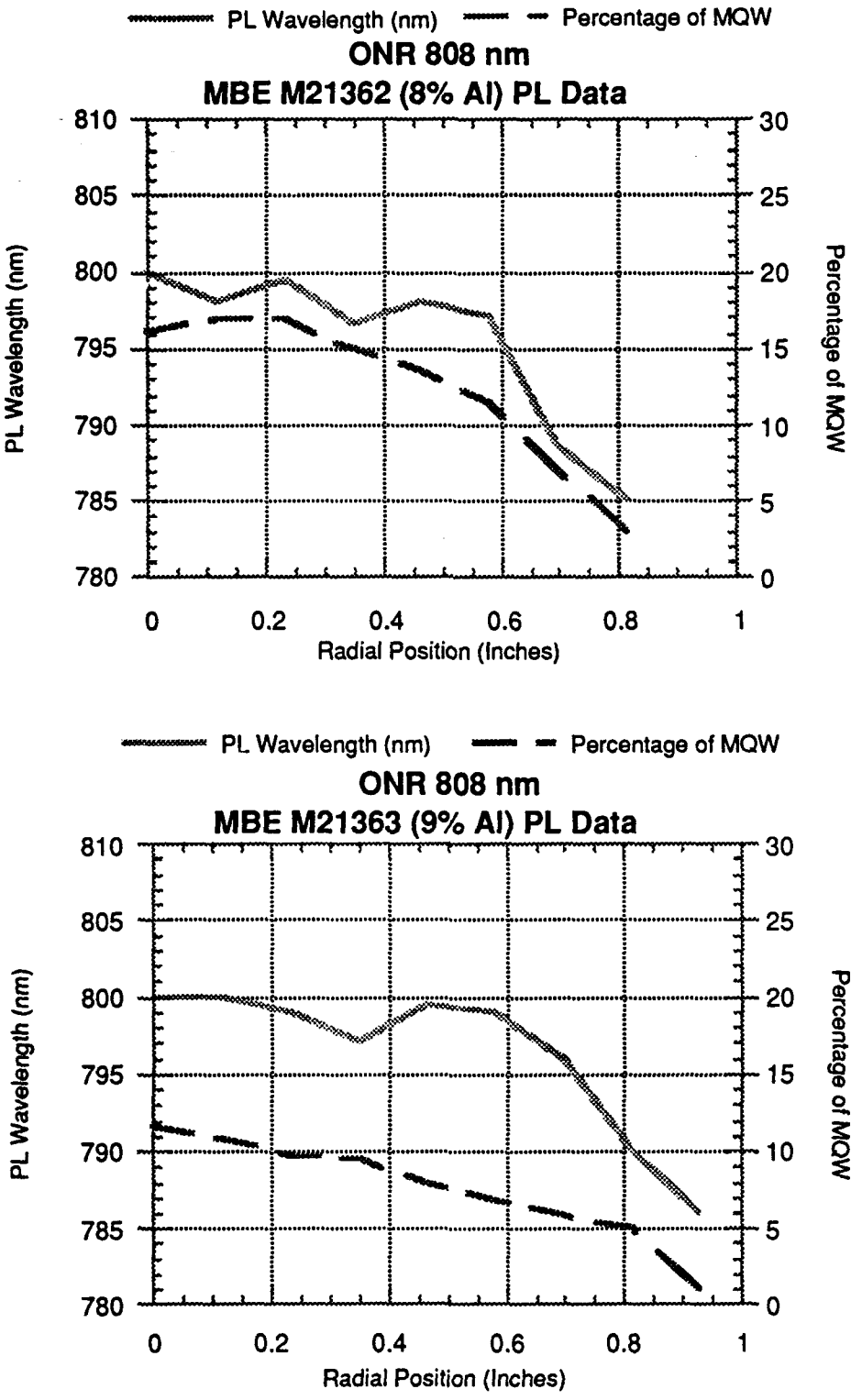
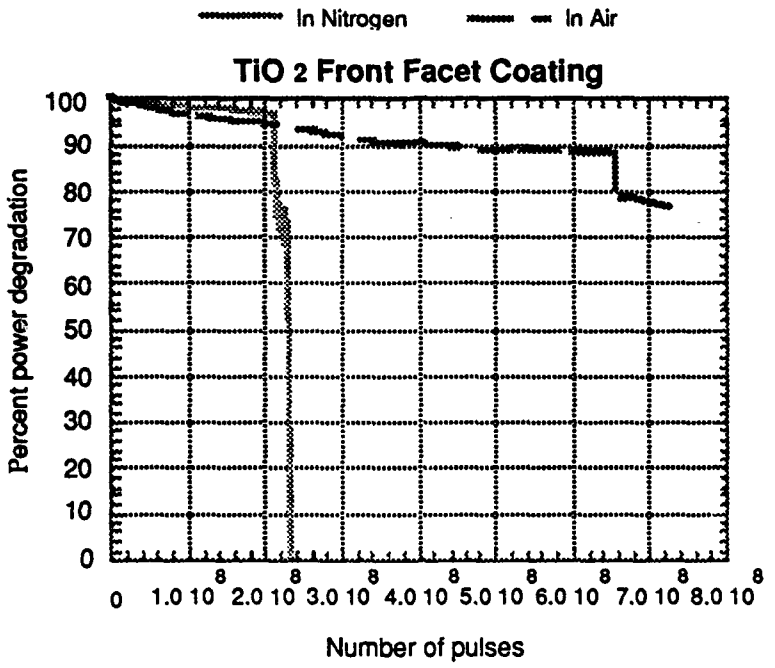
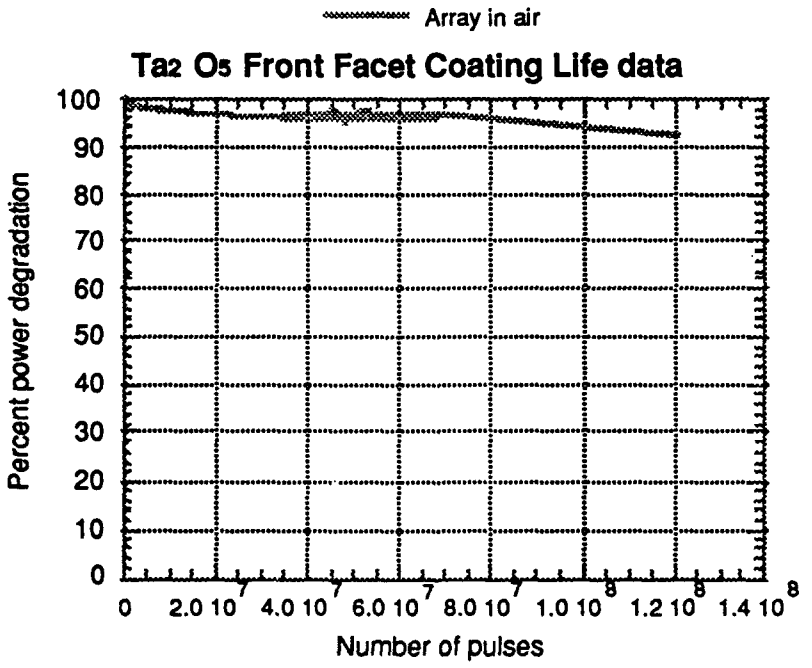


FIGURE 1 PL DATA FOR TWO WAFERS CURRENTLY BEING PROCESSED
CONTRACT NO. N00014-91-C-0222



(A)



(B)

Operating Conditions:

Duty Cycle: 2.0%
Temperature: 20°C
Current: 50 amps

FIGURE 2 LIFE-TEST DATA FOR FACET COATING EVALUATION
CONTRACT NO. N00014-91-C-0222